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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/718,344	11/20/2003	Seong-Ho Jeung	5649-966DV	1240

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MYERS BIGEL SIBLEY & SAJOVEC
PO BOX 37428
RALEIGH, NC 27627

EXAMINER	
PHUNG, ANH K	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 03/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/718,344	JEUNG, SEONG-HO	
	Examiner	Art Unit	
	ANH PHUNG	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,11,12,14,17,21 and 22* is/are rejected.

7)☒ Claim(s) *9,10,13,15,16 and 18-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/123,601.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *Nov. 20, 2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *Attachment A: Search History*. & Attached Figure 3

DETAILED ACTION

1. In response to the Application Serial No. **10/718,344** filed on November 20, 2003, claims 1-22 are pending in the application.

Priority

2. Applicant is reminded that in order for a patent issuing on the instant application to obtain the benefit of priority based on priority papers filed in parent Application No. **10/123,601** under 35 U.S.C. 119(a)-(d) or (f), a claim for such foreign priority must be made in this application. In making such claim, applicant may simply identify the application containing the priority papers.

Information Disclosure Statement

3. This office acknowledges receipt of the following items from the Applicant:

Information Disclosure Statement (IDS) filed November 20, 2003.

Information disclosed and listed on PTO 1449 was considered.

Specification

4. In the specification:

Page 1, line 8, after "April 16, 2002", insert -- , **now U.S. Pat. No. 6,674,670, issued on January 6, 2004** --.

Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification. Appropriate correction is required.

Claim Objections

5. In claim **1**:

Line 1, the word "date" should be – **data** --. Correction is required.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims **1-8**, **11-12**, **14**, **17** and **21-22** are rejected under 35 U.S.C. 102(a) as being anticipated by Ngai et al. (U.S. Pat. No. 6,400,635).

Regarding claim **6**, Ngai et al. disclose in Figures 1-7, a memory device comprising a plurality of memory cells (100, Fig. 2) wherein each memory cell comprises a latch circuit (230-240, Fig. 3) having first and second complementary latch outputs (Node1 & Node 2, Fig. 3, Attached Fig. 3) and first and second write circuits (210 & 212, Fig. 3) respectively coupled to said first and second latch outputs (Node1 & Node 2, Fig. 3, Attached Fig. 3); a plurality of write word lines (132-2, Fig. 3) wherein each write word line (132-2, Fig. 3) is coupled with the first and second write circuits (210 & 212, Fig. 3) of a respective plurality of memory cells (100, Fig. 2); a plurality of complimentary write bit line pairs (112-1D & 112-2D, Fig. 3) wherein write bit lines of each complimentary write bit line pair (112-1D & 112-2D, Fig. 3) are respectively coupled with the first and second write circuits (210 & 212, Fig. 3) of a plurality of memory cells (100, Fig. 2); and a controller (130-2, Fig. 2) that selects a memory cell to which data is to be written, activates a write word line (132-2, Fig. 3) coupled to the first

and second write circuits (210 & 212, Fig. 3) of the selected memory cell to which data is to be written, and applies complementary write values to complementary write bit lines of a write bit line pair (112-1D & 112-2D, Fig. 3) coupled with the first and second write circuits (210 & 212, Fig. 3) of the selected memory cell, so that the first and second latch outputs (Node1 & Node 2, Fig. 3, Attached Fig. 3) of the selected memory cell are coupled with the complementary write bit lines of the write bit line pair (112-1D & 112-2D, Fig. 3) coupled therewith to write the complementary write values to the first and second latch outputs (Node1 & Node 2, Fig. 3, Attached Fig. 3) of the selected memory cell responsive to activating the write word line (132-2, Fig. 3) coupled to the first and second write circuits (210 & 212, Fig. 3) of the selected memory cell.

Regarding claim **7**, Ngai et al. disclose the controller (130-2, Fig. 2) applies a same value to complementary bit lines of complementary bit line pairs not coupled with the selected memory cell.

Regarding claim **8**, Ngai et al. disclose the controller (130-2, Fig. 2) applies a same high logic value to complementary write bit lines of the complementary write bit line pairs (112-1D & 112-2D, Fig. 3) not coupled with the selected memory cell.

Regarding claim **11**, Ngai et al. disclose in Figures 1-7, a memory device comprising a plurality of write word lines (132-2, Fig. 3); a plurality of complementary write bit line pairs (112-1D & 112-2D, Fig. 3); and a plurality of memory cells (100, Fig. 2) wherein each memory cell comprises a latch circuit (230-240, Fig. 3) that latches first and second complementary logic values at first and second outputs (Node1 & Node 2, Fig. 3, Attached Fig. 3) thereof, a first write circuit (210, Fig. 3) coupled between the first

latch output (Node 1, Fig. 3) and a first write bit line (112-1D, Fig. 3) of a complimentary write bit line pair (112-1D & 112-2D, Fig. 3) coupled to the memory cell, and a second write circuit (212, Fig. 3) coupled between the second latch output (Node 2, Fig. 3) and a second write bit line (112-2D, Fig. 3) of the complimentary write bit line pair (112-1D & 112-2D, Fig. 3) coupled to the memory cell, so that the first and second latch outputs (Node1 & Node 2, Fig. 3, Attached Fig. 3) are coupled to the respective first and second write bit lines of the complementary write bit line pair (112-1D & 112-2D, Fig. 3) coupled to the memory cell responsive to a write signal on the write word line (132-2, Fig. 3) coupled with the memory cell.

Regarding claim **12**, Ngai et al. disclose the first write circuit (210, Fig. 3) of a memory cell comprises a first transistor having a first source/drain coupled to the first latch output (Node 1, Fig. 3), a second source/drain coupled to the first write bit line (112-1D, Fig. 3) of the complementary write bit line pair (112-1D & 112-2D, Fig. 3), and a gate coupled to the write word line (132-2, Fig. 3), and wherein the second write circuit (212, Fig. 3) of the memory cell comprises a second transistor having a third source/drain coupled to the second latch output (Node 1, Fig. 3), a fourth source/drain coupled to the second write bit line (112-2D, Fig. 3) of the complementary write bit line pair (112-1D & 112-2D, Fig. 3), and a gate coupled to the write word line (132-2, Fig. 3).

Regarding claim **14**, Ngai et al. disclose the first voltage (Vss ground voltage) is a ground voltage, and the second voltage (Vdd power supply voltage) is a supply voltage.

Regarding claim **17**, Ngai et al. disclose a second write circuit (212, Fig. 3) for transmitting second external voltage loaded in a second write bit line (112-2D, Fig. 3) of

the at least one write bit line to the second node in response to the first write word line (132-2, Fig. 3), wherein the first external voltage and the second external voltage have logically opposite voltage levels.

Regarding claim **21**, Ngai et al. disclose the read circuit (250 or 260, Fig. 3) further comprises a fifth NMOS transistor, which has one end connected to a second read bit line (148-1 or 148-2, Fig. 3) of the at least one read bit line (148-1 or 148-2, Fig. 3) and a gate connected to a second read word line (142-1 or 142-2, Fig. 3) of the at least one read word line (142-1 or 142-2, Fig. 3); and a sixth NMOS transistor, which has one end connected to the other end of the fifth NMOS transistor, another end connected to a second virtual ground, and a gate connected to the second node.

Regarding claim **22**, Ngai et al. disclose in Figures 1-7, a semiconductor memory cell comprising a write word line (132-2, Fig. 3); a write bit line (112-1D or 112-2D, Fig. 3); a read word line (142-1 or 142-2, Fig. 3); a read bit line (148-1 or 148-2, Fig. 3); a virtual ground; a latch circuit (230-240, Fig. 3) for latching a predetermined voltage and including first and second nodes having opposite voltage levels (Vdd power supply voltage - Vss ground voltage); a write circuit (210 or 212, Fig. 3) for transmitting a first external voltage loaded in the write bit line (112-1D or 112-2D, Fig. 3) to the first node in response to a signal of the write word line (132-2, Fig. 3); and a read circuit (250 or 260, Fig. 3) for inverting the voltage level of the second node in response to a signal of the read word line (142-1 or 142-2, Fig. 3) and the virtual ground and transmitting the voltage to the read bit line (148-1 or 148-2, Fig. 3), wherein the virtual ground is ground voltage or a supply voltage which can be changed.

Claims **1-5** are rejected as being directed to the method or/and steps derived from the apparatus described in claims **6-8** and **11-14** above.

Allowable Subject Matter

8. Claims **9-10, 13, 15-16** and **18-20** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Chiu et al. (U.S. Pat. No. 5,901,079) and Chung et al. (U.S. Pat. No. 5,590,087) disclose a semiconductor memory device similar to that of Ngai et al. (U.S. Pat. No. 6,400,635).

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **ANH PHUNG** whose telephone number is **(571) 272-1883**. The examiner can normally be reached on Monday-Friday from 8:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **RICHARD ELMS**, can be reached on **(571) 272-1869**. The fax phone number for the organization where this application or proceeding is assigned is **(703) 872-9306**.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the TC2800 telephone directory whose telephone number is **(571) 272-2800**.

Art Unit: 2824

AKP

ANH PHUNG
PRIMARY EXAMINER